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(54) **Memory device and serial-parallel data transform circuit**

Speicheranordnung und serielle/parallele Datenwandlerschaltung

Dispositif de mémoire et circuit série/parallèle de transformation de données

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to a memory device and a serial-parallel data transforming circuit, and more specifically to the memory device and the serial-parallel data transforming circuit which can write data in cells at high speed in a DRAM, in particular.

BACKGROUND OF THE INVENTION

[0002] As is well known, when cell data are accessed in the DRAM, since small charge information stored in the cells must be sensed and further amplified, it takes a long time for accessing the cell data. In this case, the sensing operation must be executed for all the cells belonging to selected word lines, that is, selected rows in a cell array.

[0003] By the utilization of the sensing operation, a page mode is well known in which the cells belonging to the same row are accessed at high speed. In this page mode, bit lines and sense amplifiers connected to a number of cells are rewritten compulsorily. Therefore, there inevitably exists a speed limit in the write cycle in this page mode.

[0004] To overcome this problem, there has been known a method of executing the page mode without directly transfer data to and from the bit lines (as disclosed in Japanese Published Unexamined (Kokai) Patent Application No. 60-7690, or U.S. Patent No. 4,608,666). In this method, a row of SRAM cells is arranged along the rows of the DRAM cell array, and data are transferred between the DRAM and an external circuit through the SRAM cells. In this method, since the sense operation and the bit line capacitance of the DRAM cells can be separated from the external data transfer due to the presence of the SRAM cells, it is possible to obtain a high speed access determined by the access cycle to the SRAM.

[0005] In the above-mentioned method of accessing the DRAM via the SRAM, however, data transfer is executed between the SRAM and the DRAM in unit of row, some restriction conditions arises in the SRAM cells. In more detail, since the contents of the SRAM cells in which data are not written are undefined, when data are written in a part of the SRAM cells and further the written data are transferred to the DRAM cells, undefined data are written in the DRAM cells corresponding to the SRAM cells to which data are not written, with the result that the data so far stored in the DRAM cells are destroyed. To solve this problem, it is necessary to write data in all the SRAM cells or to transfer the contents of the DRAM cells (to which data are to be transferred) to the SRAM cells previously, before a part of the DRAM cell contents are rewritten.

[0006] The problem involved in the prior art memory device will be described in further detail hereinbelow.

[0007] In the memory device for accessing a DRAM via a SRAM, to rewrite one row of the DRAM, data of the SRAM are transferred in parallel, and data in one row of the DRAM are rewritten. In this case, where all bit data of the SRAM have been written immediately before data transfer, one row data of the DRAM are replaced with the SRAM data due to parallel transfer. However, in order to rewrite a part of the data in a row of the DRAM, when data are written in a part of bits of the SRAM and data are not written in other remaining bits of the SRAM, the bit data not written in the SRAM are not decided (either of H or L). Under these conditions, when the data are transferred from the SRAM to the DRAM as described above, data of "1" or "0" can be written correctly from the data-written bits to the corresponding bits of the DRAM for data rewrite. However, the undecided data are written from the data-undecided bits to the corresponding bits of the DRAM. Therefore, a part of data not required to be rewritten in the DRAM are written as undecided data, thus data being destroyed.

[0008] To prevent the above-mentioned problem, there are two methods as described above. One method is as follows: even when a part of bits in a row of the DRAM are required to be rewritten, all the bits of the SRAM are previously written, and all the bits of the SRAM are transferred to one row of the DRAM. The other method is as follows: as with the case of the ordinary DRAM provided with the SRAM, all the data in a row of the DRAM are transferred to the SRAM, and only a part of the bits already transferred to the SRAM are written, without writing remaining bits (left as they are). In this case, when data are transferred from the SRAM to the row of the DRAM, the rewritten data in the SRAM are transferred to the corresponding bits of the DRAM for data rewrite. The other bits of the DRAM are restored to the original data of their own. In the above-mentioned two prior art methods, however, in spite of the fact that only a part of bits in a row of the DRAM are rewritten, there exists such a problem in that it takes a long time.

[0009] As described above, in the conventional memory device, an additional time is required to transfer data from the DRAM cells to the SRAM cells. In addition, since another time required to write data in all the SRAM cells cannot be disregarded and therefore not negligible, some problems arise in that the effect of the high cycle operation is reduced and further a large limitation exists in use of the above-mentioned method.

SUMMARY OF THE INVENTION

[0010] With these problems in mind, therefore, it is the object of the present invention to provide a memory device of high speed access, by which data can be transferred from the SRAM to the DRAM after data have been written in a part of the columns in a row of the SRAM, when data are rewritten in a part of the row or when data are written at only a part of the column addresses, with-

out any special considerations for use, in such a memory device that the sensing operation related to the DRAM row access and the column access operation can be executed separately.

[0011] To achieve the above-mentioned object, the present invention provides a memory device comprising: at least one memory block having a plurality of memory cells arranged into roughly a matrix pattern, a column group being formed by a predetermined number of columns; a plurality of sense amplifiers each provided for each of the columns; a plurality of latches each provided for each of said sense amplifiers, data being transferred between each of said latches and a corresponding one of said sense amplifiers, a latch group being formed by a predetermined number of said latches, the latch group corresponding one-to-one to the column group; a column decoder for outputting a column group select signal to select a predetermined number of the latch groups, external data being written only in the selected latch groups; characterized by a plurality of write mask circuits each for storing the latch groups in which data have been written and for enabling data written in the selected latch groups to be transferred to said corresponding sense amplifiers.

[0012] Further, the present invention provides a serial-parallel data transforming circuit, comprising: serial data inputting means for receiving external serial data; latching means having a plurality of latches for latching each of the serial data, predetermined numbers of said latches constituting a plurality of latch groups, respectively for outputting data latched by said plurality of said latches as parallel data therefrom; a plurality of data transfer gates each provided at an output terminal of one of said latches; and transfer masking means for selecting any of said latch groups, writing the serial data in the latches of the selected latch group, and turning on said data transfer gates corresponding to the latch group in which data have been written to output the parallel data therefrom while keeping closed said data transfer gates corresponding to the latch group in which data have been not written.

[0013] In the memory device according to the present invention, the control means opens only the data transfer means corresponding to the latch circuits to which data have been written, so that data can be transferred from the latch circuits to the sense amplifiers. Therefore, only the necessary data are latched by the latch circuits, so that it is possible to eliminate wasteful data write to the latch circuits, thus realizing a high speed data transfer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

Fig. 1 is a schematic block diagram showing an embodiment of the memory device according to the present invention;

Fig. 1A is a part of more practical circuit shown in Fig. 1;

Fig. 2 is a detailed circuit diagram showing the essential portion related to data transfer operation in Fig. 1;

Fig. 2A is a detailed block diagram showing the even ordinal number column blocks;

Fig. 2B is a detailed block diagram showing the odd ordinal number column blocks;

Fig. 2C is a flowchart showing a data rewrite procedure according to the present invention;

Fig. 2D is a timing chart showing the operation of the data rewrite procedure shown in Fig. 2C;

Fig. 3 is a practical circuit diagram showing the byte write mask circuit block 1 shown in Figs. 1 and 2; and

Fig. 4 is a practical circuit diagram showing the byte pair read decoder 8 shown in Fig. 1.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0015] The embodiment of the memory device according to the present invention will be described hereinbelow with reference to the attached drawings.

[0016] Fig. 1 is a schematic block diagram showing an embodiment of the memory device according to the present invention, in which the circuit configuration related to only the row direction access is shown. In Fig. 1, two 256-Kbit cell blocks 11 are shown as a part of a memory cell array. Further, each cell block 11 is composed of 256 row x 1024 columns.

[0017] On both sides of each cell block 11, 512-column sense amplifiers 3 are arranged. Further, on both sides of each cell block 11, latches (SRAM cells) 2 directly accessible from the outside (whose number is equal to the sense amplifiers 3) are arranged. These latches 2 are so constructed as to be accessible for each 8 bits simultaneously, that is, in unit of byte.

[0018] As the byte data transfer path, byte data lines 4 are arranged in the vicinity of the latches 2, respectively. Further, a byte write mask circuit block 1 is provided for each latch 2, to enable data transfer between the latches 2 and the corresponding sense amplifiers 3, only when byte data are written from a byte data line 4 to the latches 2.

[0019] Between the two cell blocks 11 of 256 Kbits, column decoders 9 are provided for selecting the latches 2 in unit of byte. The column decoders 9 are used in common for both side cell blocks 11 so as to activate only one of the cell blocks 11 in divisional operation.

[0020] The latches 2 are arranged on both sides of each cell block 11. Further, on both sides of the latches 2, a byte pair read decoders 8 is arranged, respectively. The byte pair decoder 8 decides whether the both-side latches 2 are selected as a pair or only the one-side latches 2 are selected as a single. When the one-side latches 2 are selected, the numbers of the column decoders 9 corresponding to the latches 2 are n-1, n,

$n+1, \dots$ On the basis of the numbers of the column decoders 9, the selection conditions are determined. For instance, in the case of $n-1$, the latches 2 arranged on the side opposite to the column decoders 9 are selected; in the case of n , the latches 2 arranged on the same side of the column decoders 9 are selected; and so on.

[0021] Fig. 2 shows a practical circuit related to the essential portion of the data transfer in Fig. 1, in which there are shown the sense amplifiers 3, the latches 2, the byte data lines 4, the byte write mask circuit block 1, and control signals all arranged on one side (the right side in Fig. 1) of the cell block 11.

[0022] The 8 sense amplifiers 3(0) to 3(7) provided on one side of the cell block 11 are connected to the 8 latches 2(0) to 2(7) via 8 switching transistors T, respectively. On the other hand, a byte transfer signal BX applied to the gates of the switching transistors T is formed by the byte write mask circuit block 1. When this byte transfer signal BX changes to an H level in transfer, data can be written selectively for each byte in the latches 2.

[0023] The 8 latches 2 for constituting one byte are connected to the 8-pair byte data lines 4(00), 4(01) to 4(70), 4(71) via gates G, respectively. Further, data are transferred simultaneously to the latches 2 corresponding to the byte to which the select signals CSL of the selected column decoders 9 change to the H level.

[0024] When the select signal CSL changes to the H level, the byte write mask circuit block 1 stores this H level. After that, when a word transfer signal /WX changes to the L level, the byte transfer signal BX is set to the H level, so that the data already written in the latches 2 are transferred to the sense amplifiers 3, respectively.

[0025] A signal read byte /RB is used to read data from any bytes in data read, irrespective of the select signal CSL. In other words, when the signal read byte /RB is set to the L level, the byte transfer signal BX is set to the H level, to transfer data of the sense amplifiers 3 to all the latches 2, respectively.

[0026] More practical circuits shown in Figs. 1 and 2 are shown in Figs. 1A, 2A and 2B, respectively.

[0027] Fig. 1A shows a part of the circuit shown in Fig. 1. In Fig. 1A, the same reference numerals have been retained for the similar elements which have the same functions as with the case shown in Fig. 1. The cell block 11 is composed of 128-units of column blocks CB_0 to CB_{127} , and each column block is composed of 8 columns. The two adjacent column blocks CB_i and CB_{i+1} are arranged in symmetry in Fig. 1A. In more detail, the odd ordinal number column blocks CB_0, CB_2, \dots are arranged as shown in Fig. 2B, and the even ordinal number column blocks CB_1, CB_3, \dots are arranged as shown in Fig. 2A. To the respective column blocks CB_i and CB_{i+1} , the byte write mask block circuits 1_i and 1_{i+1} arranged on both sides of the column blocks are connected, respectively. The reason why the byte write mask block circuit 1 is arranged on both sides as shown in Fig. 1A is that since the size of this circuit 1 is relatively large, it is difficult to arrange this circuit only one side of

the column block. By the layout as described above, it is possible to reduce the pattern area of the device. To each byte write mask block circuit 1_i , a select signal CSL_i is applied from the column decoder 9 together with the signals /RB and /WX applied from the control circuit CC.

[0028] Fig. 2A shows the essential portion of the column block CB_1 shown in Fig. 1A, in which the column block CB_1 is composed of 8 columns C_0 to C_7 .

[0029] The read operation can be executed as follows: For instance, when a word line WL_0 is activated, data of the memory cell MC is read to the bit lines BL_0 and $/BL_0$ previously equalized by the equalizing means EQ_0 . The read data is sensed and further amplified by the sense amplifier (S/A) 3_0 . The data sensed by the sense amplifier (S/A) 3_0 is stored by a latch 2_0 via two switching transistors T_0 . The data of the latch 2_0 is transmitted to the DQ data lines $4_{(00)}$ and $4_{(01)}$ via two transfer gates G_0 . The above-mentioned switching transistors T_0 are turned on or off on the basis of the signal BX_i applied by the byte write mask circuit 1_i . The above-mentioned transfer gates G_0 are turned on or off on the basis of the select signal CSL_1 applied by the column decoder 9.

[0030] The write operation is executed as follows: The case where only data of the two column blocks CB_1 and CB_2 are rewritten will be described hereinbelow. Two 8-bit data DG_1 and DG_2 applied from the external EXT are previously written in the respective latches 2_0 to 2_7 , and 2_0 to 2_7 of the column blocks CB_1 and CB_2 via the DQ buffers DB being divided into two times (data loads 1 and 2). After that, the latched data are transferred to and stored at the respective 8-bit memory cells connected to the activated word lines of the column blocks CB_1 and CB_2 . In this transfer, the switching transistors T connected to the non-rewrite column blocks CB_0 , and CB_3 to CB_{127} (to which no data are written) are kept turned off (i.e., masked). Therefore, it is possible to prevent data in the non-rewrite column blocks from being destroyed.

[0031] The above-mentioned data write operation will be described in further detail with reference to a flow-chart shown in Fig. 2C and a timing chart shown in Fig. 2D.

(i) Data load 1 is executed (in step S1). That is, the column select signal CSL_1 is outputted to designate a column address in the column block CB_1 (at time t_0). Further, the transfer gates G are turned on, so that data (DG_1) is transferred from the DQ lines to the latch 2 and then stored thereat (at time t_0).

(ii) Data load 2 is executed (in step S2). That is, the column select signal CSL_2 is outputted to designate a column address in the column block CB_2 (at time t_1). Further, the transfer gates G are turned on, so that data (DG_2) is transferred from the DQ lines to the latch 2 and then stored thereat (at time t_1).

(iii) The word line WL is activated (in step S3, at time t_2).

(iv) Only in the column blocks CB_1 and CB_2 , the switching transistors T are turned on on the basis of the signals BX_1 and BX_2 , so that data are transferred from the latch 2 to the sense amplifiers 3 (in step S4 and at time t_3). In other column blocks CB_0 , CB_3 , ..., CB_{127} , the data transfer as described above is not executed.

(v) In the above-mentioned masked conditions, the signal /SAN is set to a low level and the signal SAP is set to a high level (in step S5 and at a time t_4). By this, data can be rewritten in only the column blocks CB_1 and CB_2 . In the other column blocks, the data read from their own column blocks are written again as they are, so that it is possible to prevent data from being destroyed at the other column blocks.

[0032] The above-mentioned control operation can be executed under control of the control circuit CC.

[0033] Fig. 3 shows a practical byte write mask circuit block 1 shown in Figs. 1 and 2. As shown in Fig. 3, the select signal CSL is inputted to the gate of an N-channel MOS transistor 20. Further, the word transfer signal /WX is given to the gates of a P-channel MOS transistor 22, an N-channel MOS transistor 26, a P-channel MOS transistor 30, and N-channel MOS transistor 31. On the other hand, the signal read byte /RB is inputted to the gate of a P-channel MOS transistor 32. Further, the source of the transistor 20 is connected to a low potential supply voltage via an N-channel MOS transistor 21. The drain of the transistor 20 is connected to a high potential supply voltage via P-channel MOS transistors 22 and 23. The drain of the transistor 20 is connected to the source of the transistor 26 via two opposite parallel connected inverter circuits 24 and 25. The drain of the transistor 26 is connected to the gates of the transistor 21 and P-channel MOS transistors 23 and 29 via two opposite parallel connected inverter circuits 27 and 28. The source of the transistor 29 is connected to the high potential supply voltage, and the drain thereof is connected to the sources of the transistors 30 and 32, respectively. Further, the source of the transistor 32 is connected to the high potential supply voltage, and the source of the transistor 31 is connected to the low potential supply voltage. Further, the byte transfer signal BX is outputted from the drains of the transistors 30 and 31. In the above-description, the two inverter circuits 24 and 25 are provided with an input-data self-holding function, which is referred to as a first register circuit RC1, hereinafter. In the same way, the two inverter circuits 27 and 28 are provided with the similar self-holding function, which is referred to as a second register circuit RC2, hereinafter.

[0034] In the circuit construction as described above, the level of the select signal CSL is held by the first register circuit RC1. The second register circuit RC2 connected in series with the first register circuit RC1 is provided to generate the byte transfer signal BX for byte latch transfer, where necessary, in response to the se-

lect signal CSL held by the transistor 26.

[0035] The first register circuit RC1 stores the H level of the select signal CS in the following two cases:

(1) The case where data are not being transferred and further where the word transfer signal /WX for transferring data to the sense amplifiers 3 is at the H level so that the transistor 26 is turned on and the transistor 22 is turned off to select the byte write mask circuit block 1 for the first time. In other words, the case where the transistor 21 is turned on and further the transistor 23 is turned off.

(2) The case where data are being transferred and further where the word transfer signal /WX is at the L level so that the transistor 26 is turned off and the transistor 22 is turned on and further where the second register circuit output is at the H level so that the transistor 23 is turned off and the transistor 21 is turned on. That is, the case of the latch to which data are not being transferred.

[0036] When data are being transferred and further the output of the second register circuit RC2 is at the L level, that is, when corresponding to the latch to which data are being now transferred, since the transistors 23 and 22 are both turned on and the transistor 21 is turned off, the status of the first register circuit RC1 is reset irrespective of the level of the select signal CSL.

[0037] Through the above-mentioned operation, data transfer is made on the basis of only the select signal CSL selected before the transfer start time point, and these latches 2 are reset to the non-select status after the data transfer. Further, the latches 2 selected during the transfer can transfer data at the succeeding data transfer, so that it is possible to guarantee the continuity of the data write in the latches 2. Further, in the memory initialization operation of resetting the first register circuit RC1, the word transfer signal /WX is changed from the H level to the L level and then returned to the H level. On the other hand, the second register circuit RC2 receives the output of the first register circuit RC1 and holds the received output as the information for outputting the byte transfer signal BX, during the period other than the data transfer. Further, the first and second register circuits RC1 and RC2 are disconnected from each other during the data transfer period by the transistor 26 on the basis of the word transfer signal /WX applied to the gate thereof.

[0038] Further, the signal read byte /RB inputted to the gate of the transistor 32 is used to change the byte transfer signal BX (as the data transfer control signal) to the H level during the data transfer period, irrespective of the status of the second register circuit RC2.

[0039] In other words, the byte write mask circuit block 1 comprises the first register circuit RC1 for storing the selection of a group of the latches 2, and the second register circuit RC1 for holding the status of the first register RC1 (connected to the second register RC2 via the

transistor (switching element) 26) as the information for forming the byte transfer signal BX. Therefore, when data are transferred to the sense amplifiers 3, the first register circuit RC1 is disconnected from the second register circuit RC2 by this switching transistor 26, so that the first register circuit RC1 can hold the status selected during this disconnection period. Further, the second register circuit RC2 can hold the status of the first register circuit RC1 immediately before data are transferred, to form the byte transfer signal BX.

[0040] Through the operation as described above, it is possible to eliminate the wasteful time related to the high speed data access, thus enabling a high-efficiency operation beyond the dynamic memory device.

[0041] Fig. 4 is a detailed block diagram showing the byte pair read decoder 8 for changing the selection mode of the latches 2 by the column decoders 9. As shown in Fig. 4, a select signal CSLn and a signal read byte RB are inputted to an NOR circuit 34 through an AND circuit 33. A select signal CSLn-1 is directly inputted to a NOR circuit 34. The output of the NOR circuit 34 is outputted as a select signals CSL via an inverter circuit 35. In the same way, a select signal CSLn+1 and a signal read byte RB are inputted to an NOR circuit 37 through an AND circuit 36. A select signal CSLn is directly inputted to a NOR circuit 37. The output of the NOR circuit 37 is outputted as another select signal CSL via an inverter circuit 38.

[0042] In other words, when byte data are read from the cell block 11, it is possible to read two continuous byte data from one cell block 11 by utilization of the byte data lines 4 arranged on both sides of the cell block 11. Further, when data written, it is of course possible to write two byte continuous data simultaneously in the same way.

[0043] As described above, the byte pair read decoder 8 is used to change-over the two-byte data read/write to the ordinary one-byte data read/write or vice versa.

[0044] Here, the one-byte mode and the two-byte mode can be switched on the basis of the signal RB (the inversion signal of the signal read byte /RB).

[0045] When the signal read byte /RB is at the L level, the select signal CSL is set to the H level even when the succeeding column decoders 9 are selected. When the column decoders 9 are selected, two continuous select signals CSL are both at the H level, so that two latches 2 can be selected.

[0046] On the other hand, when the signal read byte /RB is at the H level, only the select signals CSL corresponding to the respective column decoders 9 are at the H level.

[0047] As described above, in the memory device according to the present invention, in the dynamic memory, when data are stored temporarily by the latches 2 and then transferred to and from the cell block 11, the transfer gates inter-posed between the cell block 11 and the sense amplifiers 3 are controlled independently for each group of at least two latches 2. Further, the byte

write mask circuit blocks 1 for the above-mentioned control are arranged for each group of the latches 2. When the data are transferred to the sense amplifiers 3, the data transfer can be executed only in the group of the latches 2 in which data are written, but the data transfer cannot be executed in the group of the latches 2 in which data are not written by keeping the transfer gates closed. By doing this, it is possible to improve the access speed of the dynamic memory markedly.

[0048] Further, in the memory device according to the present invention, since the byte data are inputted in series and further these byte data are transferred to the DRAM in parallel at a time, it is possible to regard the latches 2 and the byte write mask circuit blocks 11, etc. as a serial-parallel data transforming circuit so constructed that the data outputs can be controlled for each data block.

[0049] In other words, in the serial-parallel data transforming circuit such that data are inputted in series to the latches 2 corresponding to each data group in series and further these data of the latches 2 are outputted simultaneously for data transfer, the construction is such that the transfer gates are provided to output parallel data in such a way that the transfer gates can be controlled independently for each group of a plurality of latches 2 and further the byte write mask circuit block 1 for this control is provided for each group of the latches 2. Therefore, when the parallel data are outputted, the data transfer is controlled in such a way that data are transferred to and from only the group of the latches 2 to which data have been written, and data are not transferred to and from only the group of the latches 2 to which data have not been written. The above-mentioned function can be regarded as that only the latches 2 to which data are inputted in series can function the serial-parallel data transforming circuit.

[0050] In the construction as described above, since the data transfer efficiency can be improved markedly in the serial-parallel data transforming circuit, when this construction is applied to the dynamic memory device, it is possible to increase the data transfer speed markedly.

[0051] As described above, in the DRAM of the type such that the SRAM is interposed to transfer data at high speed to and from the memory cells continuously during the data transfer period, in the memory device according to the present invention, since only any determined data can be transferred to and from the memory cells, it is possible to realize a high speed access in the DRAM.

[0052] In the memory device according to the present invention, since data are outputted from only the latch circuits (to which data have been written) and then transferred to the sense amplifier circuits, it is possible to eliminate the data write of the latch circuits corresponding to the bits (to which no data write are necessary), thus realizing the high speed access. Further, in the serial-parallel data transforming circuit according to the present invention, since data of only the latch circuits

(to which serial data are written) are parallel transformed and then outputted, the transforming efficiency can be increased.

Claims

1. A memory device comprising:

at least one memory block (11) having a plurality of memory cells arranged into roughly a matrix pattern, a column group being formed by a predetermined number of columns;
a plurality of sense amplifiers (3) each provided for each of the columns;
a plurality of latches (2) each provided for each of said sense amplifiers (3), data being transferred between each of said latches (2) and a corresponding one of said sense amplifiers (3), a latch group being formed by a predetermined number of said latches (2), the latch group corresponding one-to-one to the column group;
a column decoder (9) for outputting a column group select signal (CSL) to select a predetermined number of the latch groups, external data being written only in the selected latch groups;

characterized by a plurality of write mask circuits (1) each for storing the latch groups in which data have been written and for enabling data written in the selected latch groups to be transferred to said corresponding sense amplifiers (3).

2. The memory device of claim 1, wherein a transfer gate (T) is connected between each of said sense amplifiers (3) and each of said latches (2), a transfer gate group being formed by a predetermined number of the transfer gates (T), each of the transfer gate groups corresponding to each of the latch groups, and each of said write mask circuit (1) turning on/off one of said transfer gate groups.

3. The memory device of claim 1 or 2, wherein each of said latches (2) is connected to each of data lines (4) to transfer data to and from the outside, gating means (G) being connected between each of said latches (2) and each of the data lines (4) to turn on/off interconnection between each of said latches (2) and each of the data lines (4), a gating means group being formed by a predetermined number of said gating means (G), and each of said gating means group being selectively turned on by said column decoder (9).

4. The memory device of claim 1 or 2, which further comprises plural column group simultaneous accessing means (8) for receiving the column group

select signal given by said column decoder (9) and for outputting another select signal to select a predetermined number of column groups adjacent to the column group corresponding to the received column group select signal (CSL), so that whenever the column group select signal for selecting a column group is outputted by said column decoder, a predetermined number of column groups adjacent to the selected column group being accessed simultaneously.

5. The memory device of claim 1, which further comprises plural column group simultaneous accessing means (8) and wherein when receiving the column group select signal (CSL) given by said column decoder (9), said plural column group simultaneous accessing means (8) selects one column group adjacent to the column group corresponding to the received column group select signal (CSL) to enable simultaneous access to the two column groups.

6. The memory device of claim 5, wherein said plural column group simultaneous accessing group (8) is a column group pair read decoder.

7. The memory device of claim 5, wherein said plural column group simultaneous accessing group (8) is a column group pair write decoder.

8. The memory device of claim 5, wherein said plural column group simultaneous accessing group (8) is a column group pair read/write decoder.

9. The memory device of claim 1, 3, 4 or 5, wherein said write mask circuit (1) comprises;

a first register circuit (RC1), when the latch group corresponding thereto is selected and thereby data are written, for storing the selection at a selected time point;

a second register circuit (RC2) connected in series to said first register circuit (RC1) via a switching element (26), for storing the information stored in said first register (RC1) as information for generating a signal for controlling the transfer gate (T);

when data is transferred from said latch (2) to said sense amplifier (3), the switching element (26) being turned off to disconnect said first register circuit (RC1) from said second register circuit (RC2), while keeping the selection of the latch group under this disconnected status stored in said first register circuit; and
data stored in said first register circuit (RC1) immediately before the data transfer being outputted to said second register circuit (RC2) as the information for generating the signal for controlling the transfer gate (T).

10. The memory device of claim 1,2,3,4 or 5, wherein said memory cell block (11) is arranged in middle of the device; said sense amplifiers (3), said latches (2) and said write mask circuits (1) are arranged in sequence on both sides of said block (11) so as to sandwich said block in symmetrical positional relationship with respect to each other; and said column decoder (9) is arranged outside of one of said write mask circuits (1).

11. The memory device of claim 1, 2, 3, 4 or 5, wherein two of said memory cell blocks are provided; said column decoder (9) is arranged in middle between said two memory cell blocks (11, 11); and said write mask circuits (1), said latches (2) and said sense amplifiers (3) are arranged in sequence on both sides of said column decoder (9) so as to sandwich said column decoder (9).

12. A serial-parallel data transforming circuit, comprising:

serial data inputting means (4, G) for receiving external serial data;
latching means having a plurality of latches (2) for latching each of the serial data, predetermined numbers of said latches (2) constituting a plurality of latch groups, respectively for outputting data latched by said plurality of said latches (2) as parallel data therefrom;
a plurality of data transfer gates (T) each provided at an output terminal of one of said latches (2); and
transfer masking means for selecting any of said latch groups, writing the serial data in the latches of the selected latch group, and turning on said data transfer gates (T) corresponding to the latch group in which data have been written to output the parallel data therefrom while keeping closed said data transfer gates (T) corresponding to the latch group in which data have been not written.

13. A method for writing data to a memory device having a plurality of column lines each having memory cells (MC), connected thereto and each further having, a sense amplifier (3), a first gate (T), a latch (2), a second gate (G) and a data line (4) serially connected in this order thereto, comprising:

first step of writing data from one of said data lines (4) to one of said latches (2) corresponding to the data line (4) by turning on the second gate (G) on the basis of a column group select signal outputted from a column decoder (9) and storing in a mask means (1) column location corresponding to the column line connected to the latch (2) in which the data is written;

second step of activating a word line (WL) to transfer data stored in the memory cells (MC) to the plurality of column lines (BL);
third step of turning on only the first gate (T) connected to the written latch (2) and not turning on the first gates (T) connected to the unwritten latches (2) on the basis of a signal (BX) outputted from the mask means (1); and
fourth step of activating the sense amplifiers (3),

wherein the data from the data line (4) is written only in the memory cell (MC) corresponding to the written latch (2) and the data read from the remaining memory cells (MC) are rewritten so as not to destroy the data stored therein.

Patentansprüche

1. Speichereinrichtung, enthaltend:

mindestens einen Speicherblock (11) mit mehreren Speicherzellen, die grob in ein Matrixmuster angeordnet sind, derart, daß eine Spaltengruppe durch eine vorgegebene Zahl der Spalten gebildet ist;

mehrere Leseverstärker (3), die jeweils für jede der Spalten vorgesehen sind;

mehrere Latchelemente (2), die jeweils für jeden der Leseverstärker (3) vorgesehen sind, derart, daß Daten zwischen jedem der Latchelemente (2) und einem zugeordneten der Leseverstärker (3) transferiert werden, eine Latchelementgruppe durch eine vorgegebene Zahl der Latchelemente (2) gebildet ist, und die Latchelementgruppe in einer Eins-zu-Eins-Zuordnung zu der Spaltengruppe vorliegt;

Ein Spaltendecoder (9) zum Ausgeben eines Spaltengruppen-Auswahlsignals (CSL) zum Auswählen einer vorgegebenen Zahl der Latchgruppen, derart, daß externe Daten lediglich für die ausgewählten Latchelementgruppen geschrieben werden;

gekennzeichnet durch

mehrere Schreibmaskierungen-Schaltungen (1) jeweils zum Speichern der Latchelementgruppen, in die Daten geschrieben sind und zum Freigeben des Datenschreibens in die ausgewählte Latchelementgruppe zum Transferieren zu den zugeordneten Leseverstärkern (3).

2. Speichereinrichtung nach Anspruch 1, dadurch gekennzeichnet, daß ein Transfergate (T) zwischen jedem der Leseverstärker (3) und jedem der Latchelemente (2) angeschlossen ist, daß eine Transfergatengruppe durch eine vorgegebene Zahl der Transfergates (T) gebildet ist, derart, daß jede der Transfergatengruppe jeder der Latchelementgruppen zugeordnet ist und jeder der Schreibmaskierungsschaltungen (1) eine der Transfergatengruppen an/abschaltet. 5
3. Speichereinrichtung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß jedes der Latchelemente (2) mit jeder der Datenleitungen (4) zum Transferieren von Daten zu und von der Außenseite verbunden ist, daß Gatevorrichtungen (G) zwischen jedem der Latchelemente (2) und jeder der Datenleitungen (4) zum An/Abschalten der Verbindung zwischen jedem der Latchelemente (2) und jeder der Datenleitungen (4) angeschlossen sind, daß eine Gate-Vorrichtungsguppe durch eine vorgegebene Zahl der Gate-Vorrichtungen (G) gebildet ist und jeder der Gate-Vorrichtungsguppen selektiv durch den Spaltendecoder (9) angeschaltet ist. 20
4. Speichereinrichtung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß sie ferner mehrere Vorrichtung für den gleichzeitigen Zugriff auf die Spaltengruppen 8 enthält, zum Empfangen des Spaltengruppen-Auswahlsignals, das durch den Spaltendecoder (9) vorgegeben ist, und zum Ausgeben eines anderen Auswahlsignals zum Auswählen einer vorgegebenen Zahl der Spaltengruppen in Nachbarschaft zu der Spaltengruppe gemäß dem empfangenden Spaltengruppen-Auswahlsignal (CSL) derart, daß immer dann, wenn das Spaltengruppen-Auswahlsignal zum Auswählen einer Spaltengruppe durch den Spaltendecoder ausgegeben ist, ein gleichzeitiger Zugriff auf eine vorgegebene Zahl von Spaltengruppen in der Nähe der ausgewählten Spaltengruppe erfolgt. 30
5. Speichereinrichtung nach Anspruch 1, dadurch gekennzeichnet, daß sie ferner eine Vorrichtung für den gleichzeitigen Zugriff auf die Spaltengruppen (8) enthält, derart, daß bei Empfang des durch den Spaltendecoder (9) abgegebenen Spaltengruppen-Auswahlsignals (CSL) die Vorrichtung für den gleichzeitigen Zugriff auf die mehreren Spaltengruppen (8) eine Spaltengruppe in der Nachbarschaft der Spaltengruppe gemäß dem empfangenen Spaltengruppen-Auswahlsignal (CSL) auswählt, damit der gleichzeitige Zugriff auf die beiden Spaltengruppen ermöglicht ist. 40
6. Speichereinrichtung nach Anspruch 5, dadurch gekennzeichnet, daß die Vorrichtung für den gleichzeitigen Zugriff auf die Spaltengruppe (8) ein Lese-

decoder für ein Spaltengruppenpaar ist.

7. Speichereinrichtung nach Anspruch 5, dadurch gekennzeichnet, daß die Vorrichtung für den gleichzeitigen Zugriff auf die Spaltengruppe (8) ein Schreibdecoder für ein Spaltengruppenpaar ist. 5
8. Speichereinrichtung nach Anspruch 5, dadurch gekennzeichnet, daß die Vorrichtung für den gleichzeitigen Zugriff auf die Spaltengruppe (8) ein Lese/Schreibdecoder für ein Spaltengruppenpaar ist. 10
9. Speichereinrichtung nach Anspruch 1, 3, 4 oder 5, dadurch gekennzeichnet, daß die Schreibmaskierungsschaltung (1) enthält: 15
 - eine erste Registerschaltung (RC1) zum Speichern der Auswahl in einem vorgegebenen Zeitpunkt dann, wenn die dieser zugeordnete Latchgruppe ausgewählt ist und hierdurch Daten geschrieben sind;
 - eine zweite Registerschaltung (RC2), die in Serie zu der ersten Registerschaltung (CR1) über ein Schaltelement (26) angeschlossen ist, und zwar zum Speichern der Information, die in dem ersten Register (RC1) gespeichert ist, als Information zum Erzeugen eines Signals zum Steuern des Transfergates (T); derart, daß
 - dann, wenn Daten von dem Latchelement (2) zu dem Leseverstärker (3) transferiert werden, das Schaltelement (26) zum Abtrennen der ersten Registerschaltung (CR1) von der zweiten Registerschaltung (CR2) abgetrennt ist, unter Beibehaltung des Speicherns der Auswahl der Latchgruppe in diesem abgetrennten Status in der ersten Registerschaltung; und
 - Daten, die in der ersten Registerschaltung (CR1) unmittelbar vor dem Datentransfer gespeichert sind, zu der zweiten Registerschaltung (CR2) als Information zum Erzeugen des Signals zum Steuern des Transfergates (T) ausgegeben werden.
10. Speichereinrichtung nach Anspruch 1, 2, 3, 4 oder 5, dadurch gekennzeichnet, daß der Speicherzellblock (11) in der Mitte der Einrichtung ausgebildet ist; derart, daß die Leseverstärker (3), die Latchelemente (2) und die Schreibmaskierungsschaltungen (1) in Folge an beiden Seiten des Blocks (11) so angeordnet sind, daß sie den Block in symmetrischer Positionsbeziehung relativ zueinander in Sandwichstruktur umgeben; und der Spaltendecoder (9) an der Außenseite einer der Schreibmaskierungsschaltungen (1) angeordnet ist. 55

11. Speichereinrichtung nach Anspruch 1, 2, 3, 4 oder 5, dadurch gekennzeichnet, daß zwei der Speicherzellenblöcke vorgesehen sind; derart, daß der Spaltendecoder (9) in der Mitte zwischen zwei Speicherzellenblöcken (11, 11) angeordnet ist; und die Schreibmaskierschaltung (1) die Latchelemente (2) und die Leseverstärker (3) in Folge auf beiden Seiten des Spaltendecoders (9) so angeordnet sind, daß sie den Spaltendecoder (9) in Sandwichstruktur umfassen.

12. Serien/Parallel-Datentransformierschaltung, enthaltend:

eine serielle Dateneingabevorrichtung (4, G) zum Empfangen externer serieller Daten;

eine Latchvorrichtung mit mehreren Latchelementen (2) zum Latchen jeder der seriellen Daten, derart, daß eine vorbestimmte Zahl der Latchelemente (2) eine Vielzahl von Latchgruppen bilden, die jeweils zum Ausgeben von durch die mehreren Latchelemente (2) gehaltenen Daten als Paralleldaten ausgehend hiervon vorgesehen sind;

mehrere Datentransfergates (T), die jeweils bei einem Ausgangsanschluß gemäß der Latchelemente (2) vorgesehen sind; und

eine Transfermaskierungsvorrichtung zum Auswählen irgendeiner der Latchgruppen, zum Schreiben der seriellen Daten in die Latchelemente der ausgewählten Latchgruppe und zum Anschalten der Datentransfergates (T) in Zuordnung zu der Latchgruppe, in die Daten geschrieben sind, und zwar zum Ausgeben der parallelen Daten hiervon bei Beibehaltung des Datentransfergates (T) gemäß der Latchgruppe, in die Daten geschrieben sind, in geschlossenem Zustand.

13. Verfahren zum Schreiben von Daten zu einer Speichereinrichtung mit mehreren Spaltenleitungen jeweils mit Speicherzellen (MC), die hiermit verbunden sind, und jeweils ferner einem Leseverstärker (3), einem ersten Gate (T), einem Latchelement (2), einem zweiten Gate (G) und Datenleitungen (4), die seriell in dieser Folge hieran angeschlossen sind, enthaltend:

einen ersten Schritt zum Schreiben von Daten ausgehend von einer der Datenleitungen (4) zu einem der Latchelemente (2) in Zuordnung zu der Datenleitung (4) durch Anschalten des zweiten Gates (G) auf der Grundlage des Spaltengruppenauswahlsignals, das von einem Spaltendecoder (9) ausgegeben wird, ferner

zum Speichern in einer Maskierungsvorrichtung (1) der Spaltenstelle gemäß der mit dem Latchelement (2), in dem Daten geschrieben sind, verbundenen Spaltenleitung;

einen zweiten Schritt zum Aktivieren einer Wortleitung (WL) zum Transferieren von in den Speicherzellen (MC) gespeicherten Daten zu mehreren Spaltenleitungen (BL);

einen dritten Schritt zum Anschalten lediglich des ersten Gates (T), das mit dem Schreiblatchelement (2) verbunden ist, sowie nicht zum Anschalten der ersten Gates (T), die mit den nicht geschriebenen Latchelementen (2) verbunden sind, auf der Grundlage eines durch die Maskierungsvorrichtung (1) ausgegebenen Signals (BX); und

einen vierten Schritt zum Aktivieren der Leseverstärker (3); derart, daß die Daten von der Datenleitung (4) lediglich in die Speicherzelle (MC) geschrieben werden, die dem beschriebenen Latchelement (2) zugeordnet ist, und die von den verbleibenden Speicherzellen (MC) gelesenen Daten erneut so geschrieben werden, daß die hierin gespeicherten Daten nicht zerstört werden.

Revendications

1. Dispositif de mémoire comprenant:

au moins un bloc de mémoire (11) présentant plusieurs cellules de mémoire agencées grossièrement selon une configuration en matrice, un groupe de colonnes étant formé par un nombre prédéterminé de colonnes; plusieurs amplificateurs de détection (3) prévus chacun pour chaque colonne; plusieurs dispositifs de maintien (2) prévus chacun pour chaque amplificateur de détection (3), des données étant transférées entre chacun des dispositifs de maintien (2) et un amplificateur de détection (3) correspondant, un groupe de dispositifs de maintien étant formé par un nombre prédéterminé desdits dispositifs de maintien (2), le groupe de dispositifs de maintien correspondant de manière univoque au groupe de colonnes; un décodeur de colonne (9) pour délivrer un signal de sélection d'un groupe de colonnes (CSL) pour sélectionner un nombre prédéterminé des groupes de dispositifs de maintien, des données externes n'étant écrites que dans les groupes de dispositifs de maintien sélectionnés;

- caractérisé par plusieurs circuits (1) de masquage en écriture, pour conserver chacun les groupes de dispositifs de maintien dans lesquels des données ont été écrites, et valider le transfert de données écrites dans les groupes de dispositifs de maintien sélectionnés, aux amplificateurs de détection (3) correspondants.
2. Dispositif de mémoire selon la revendication 1, dans lequel une porte de transfert (T) est connectée entre chacun des amplificateurs de détection (3) et chacun des dispositifs de maintien (2), un groupe de portes de transfert étant formé par un nombre prédéterminé des portes de transfert (T), chacun des groupes de portes de transfert correspondant à chacun des groupes de dispositifs de maintien, et chacun desdits circuits (1) de masquage en écriture activant/désactivant l'un desdits groupes de portes de transfert.
 3. Dispositif de mémoire selon la revendication 1 ou 2, dans lequel chacun des dispositifs de maintien (2) est connecté à chacune parmi des lignes de données (4), pour transférer des données vers, et depuis l'extérieur, des moyens de porte (G) étant connectés entre chacun desdits dispositifs de maintien (2) et chacune des lignes de données (4) pour activer/désactiver l'interconnexion entre chacun desdits dispositifs de maintien (2) et chacune des lignes de données (4), un groupe de moyens de porte étant formé par un nombre prédéterminé desdits moyens de porte (G), et chacun desdits groupes de moyens de porte étant sélectivement activé par ledit décodeur de colonne (9).
 4. Dispositif de mémoire selon la revendication 1 ou 2, qui comprend de plus des moyens (8) d'accès simultané à plusieurs groupes de colonnes pour recevoir le signal de sélection de groupe de colonnes fourni par ledit décodeur de colonne (9) et pour délivrer un autre signal de sélection pour sélectionner un nombre prédéterminé de groupes de colonnes adjacents au groupe de colonnes correspondant au signal (CSL) de sélection de groupe de colonnes reçu, de telle sorte que chaque fois que le signal de sélection de groupe de colonnes pour sélectionner un groupe de colonnes est délivré par ledit décodeur de colonnes, un nombre prédéterminé de groupes de colonnes adjacents au groupe de colonnes sélectionné est sollicité simultanément.
 5. Dispositif de mémoire selon la revendication 1, qui comprend de plus des moyens (8) d'accession simultanée à plusieurs groupes de colonnes et dans lequel, lorsqu'il reçoit le signal de sélection de groupe de colonnes (CSL) donné par ledit décodeur de colonne (9), ledit moyen (8) d'accession simultanée à plusieurs groupes de colonnes choisit un groupe de colonnes adjacent au groupe de colonnes correspondant au signal de sélection de groupe de colonnes reçu (CSL), pour valider un accès simultané aux deux groupes de colonnes.
 6. Dispositif de mémoire selon la revendication 5, dans lequel le moyen (8) d'accession simultanée à plusieurs groupes de colonnes est un décodeur en lecture de paires de groupes de colonnes.
 7. Dispositif de mémoire selon la revendication 5, dans lequel ledit moyen (8) d'accession simultanée à plusieurs groupes de colonnes est un décodeur de lecture de paires de groupes de colonnes.
 8. Dispositif de mémoire selon la revendication 5, dans lequel ledit moyen (8) d'accession simultanée à plusieurs groupes de colonnes est un décodeur de lecture/écriture de paires de groupes de colonnes.
 9. Dispositif de mémoire selon la revendication 1, 3, 4 ou 5, dans lequel ledit circuit de masquage en écriture (1) comprend:
 - un premier circuit de registre (RC1) pour conserver la sélection à un instant choisi, lorsque le groupe de dispositifs de maintien y relié est choisi et que des données sont ainsi écrites;
 - un second circuit de registre (RC2) relié en série avec le premier circuit de registre (RC1) par l'intermédiaire d'un élément de commutation (26), pour conserver l'information mémorisée dans ledit premier registre (RC1) en tant qu'information pour générer un signal pour commander la porte de transfert (T);
 - lorsque des données sont transférées depuis ledit dispositif de maintien (2) audit amplificateur de détection (3) alors que l'élément de commutation (26) est désactivé pour déconnecter ledit premier circuit de registre (RC1) dudit second circuit de registre (RC2) tout en maintenant la sélection du groupe de dispositifs de maintien dans cet état de déconnexion mémorisé dans ledit premier circuit de registre; et les données conservées dans ledit premier circuit de registre (RC1) immédiatement avant le transfert de données étant délivré audit second circuit de registre (RC2) en tant qu'information pour générer le signal pour commander la porte de transfert (T).
 10. Dispositif de mémoire selon la revendication 1, 2, 3, 4 ou 5, dans lequel ledit bloc (11) de cellules de mémoire est disposé au milieu du dispositif; lesdits amplificateurs de détection (3), lesdits dispositifs de maintien (2) et lesdits circuits (1) de masquage en écriture (1) sont agencés en séquence de part et

d'autre dudit bloc (11) de façon à intercaler entre eux ledit bloc dans une relation de position symétrique l'un par rapport à l'autre; et ledit décodeur de colonne (9) est agencé à l'extérieur de l'un desdits circuits de masquage en écriture (1).

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11. Dispositif de mémoire selon la revendication 1, 2, 3, 4 ou 5, dans lequel deux desdits blocs de cellules sont prévus; ledit décodeur de colonne 9 est agencé au milieu entre les deux blocs de cellules de mémoires (11, 11); et, dans lesdits circuits de masquage en écriture (1), lesdits dispositifs de maintien (2) et lesdits amplificateurs de détection (3) sont disposés en séquence de part et d'autre dudit décodeur de colonne (9) de manière à intercaler entre eux ledit décodeur de colonne (9).

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12. Circuit de transformation série-parallèle de données, comprenant:

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des moyens d'entrée (4, G) de données série pour recevoir des données série externes; des moyens de maintien présentant plusieurs dispositifs de maintien (2) pour conserver chacune des données série, des nombres prédéterminés desdits dispositifs de maintien (2) constituant plusieurs groupes de dispositifs de maintien, pour délivrer respectivement des données conservées par ladite pluralité desdits dispositifs de maintien (2) sous la forme de données parallèles à partir de ceux-ci; et plusieurs portes (T) de transfert de données prévues chacune à une borne de sortie de l'un desdits dispositifs de maintien (2); et un moyen de masquage de transfert pour sélectionner l'un quelconque des groupes de dispositifs de maintien, écrire les données série dans les dispositifs de maintien du groupe de dispositifs de maintien sélectionné, et activer lesdites portes (T) de transfert de données correspondant au groupe de dispositifs de maintien dans lequel des données ont été écrites, pour délivrer les données parallèles à partir de celui-ci tout en maintenant fermées lesdites portes (T) de transfert de données correspondant au groupe de dispositifs de maintien dans lequel des données n'ont pas été écrites.

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13. Procédé pour écrire des données dans un dispositif de mémoire auquel sont connectées plusieurs colonnes présentant chacune des cellules de mémoire (MC), et possédant de plus un amplificateur de détection (3), une première porte (T), un dispositif de maintien (2), une seconde porte (G) et une ligne de données (4) y connectée en série, dans cet ordre, comprenant:

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une première étape consistant à écrire des

données à partir de l'une des lignes de données (4) sur l'un des dispositifs de maintien (2) correspondant à la ligne de données (4) en activant la seconde porte (G) sur base d'un signal de sélection de groupe de colonnes délivré par un décodeur de colonne (9), et conserver dans un moyen de masquage (1) une localisation de colonne correspondant à la ligne de colonnes connectée au dispositif de maintien (2) dans lequel les données sont écrites;

une seconde étape d'activation d'une ligne de mot (WL) pour transférer des données conservées dans les cellules de mémoire (MC) aux plusieurs lignes de colonnes (BL);

une troisième étape consistant à n'activer que la première porte (T) connectée au dispositif de maintien (2) qui a reçu l'écriture, et à ne pas activer les premières portes (T) connectées aux dispositifs de maintien (2) qui n'ont pas reçu d'écriture, sur base d'un signal (BX) délivré par le moyen de masquage (1); et une quatrième étape d'activation des amplificateurs de détection (3),

dans lequel les données provenant de la ligne de données (4) sont écrites uniquement dans la cellule de mémoire (MC) correspondant au dispositif de maintien (2) ayant reçu l'écriture, et les données lues à partir des cellules de mémoire (MC) restantes sont ré-écrites de façon à ne pas détruire les données qui y sont conservées.

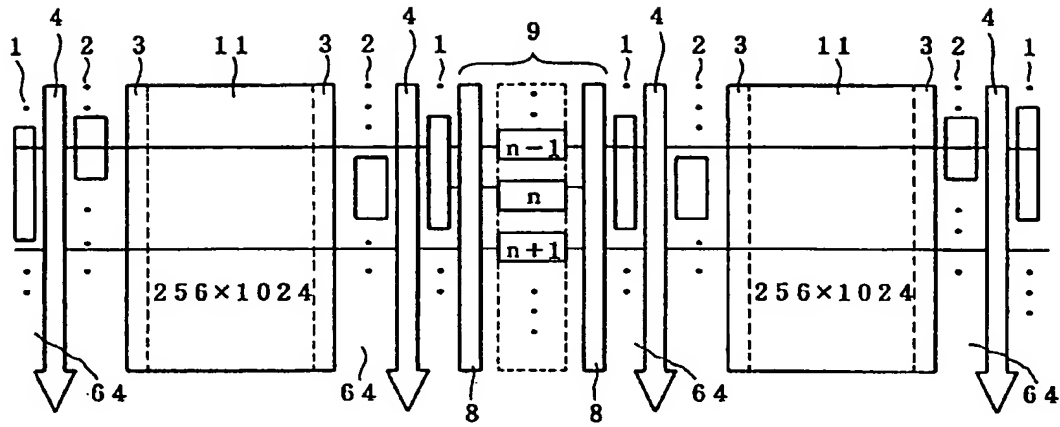


FIG. 1

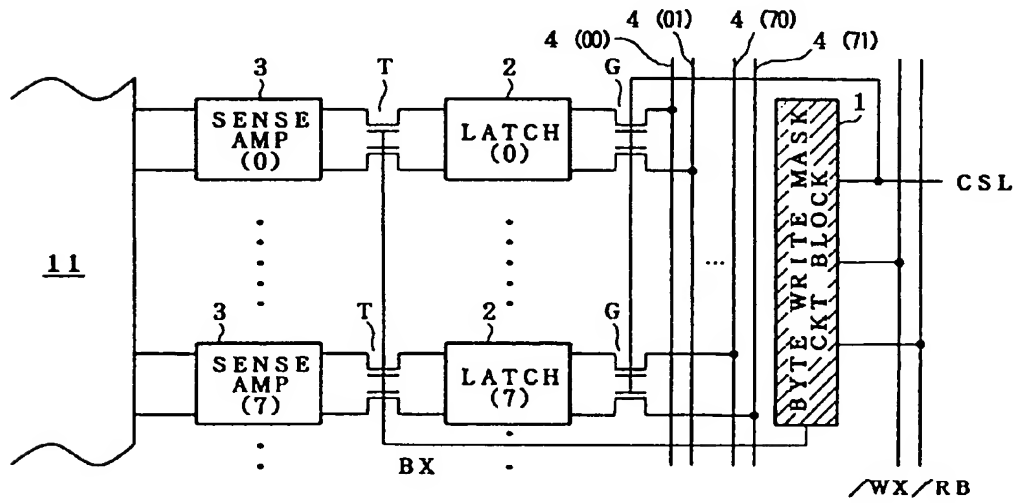


FIG. 2

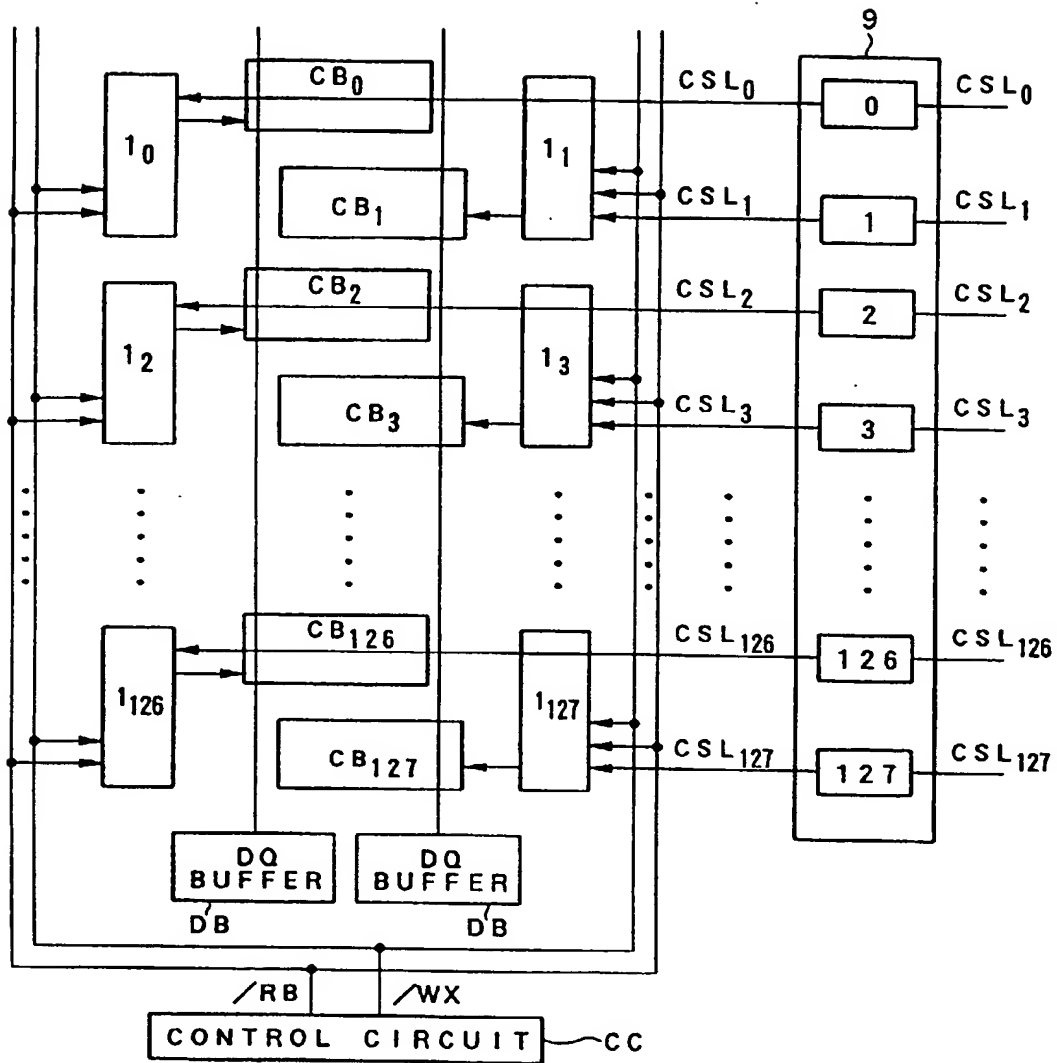


FIG. 1A

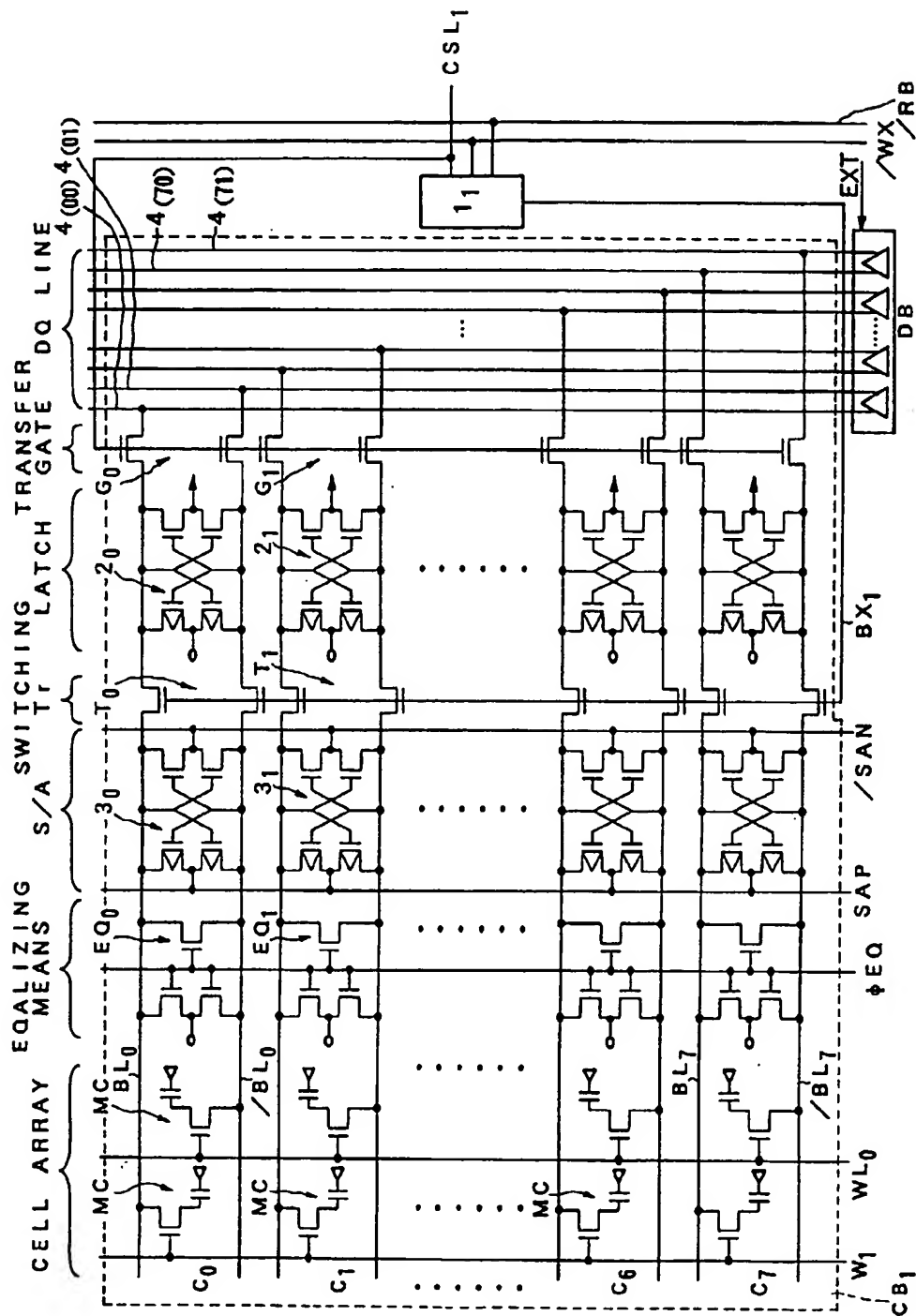


FIG. 2A

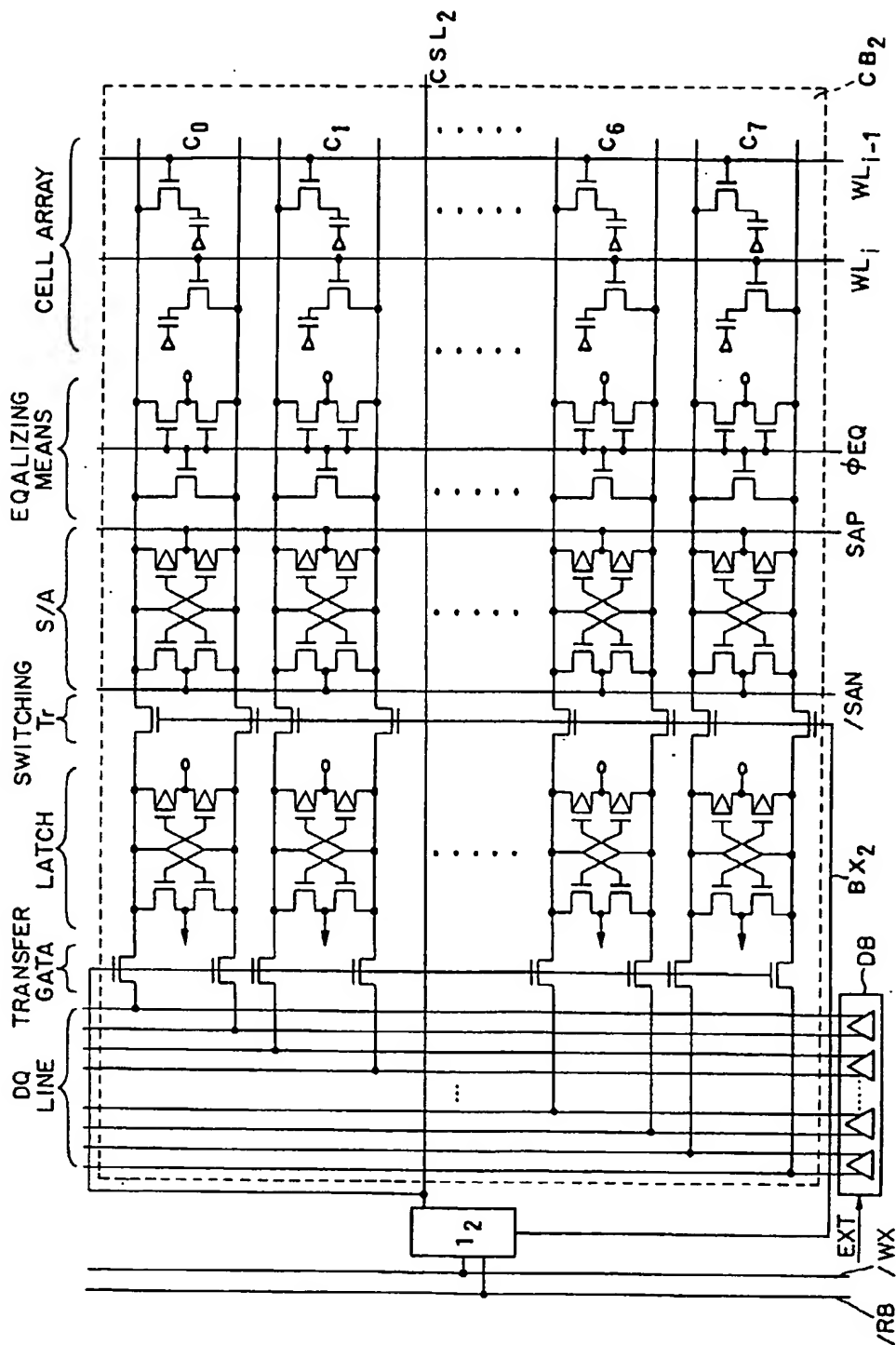


FIG. 2B

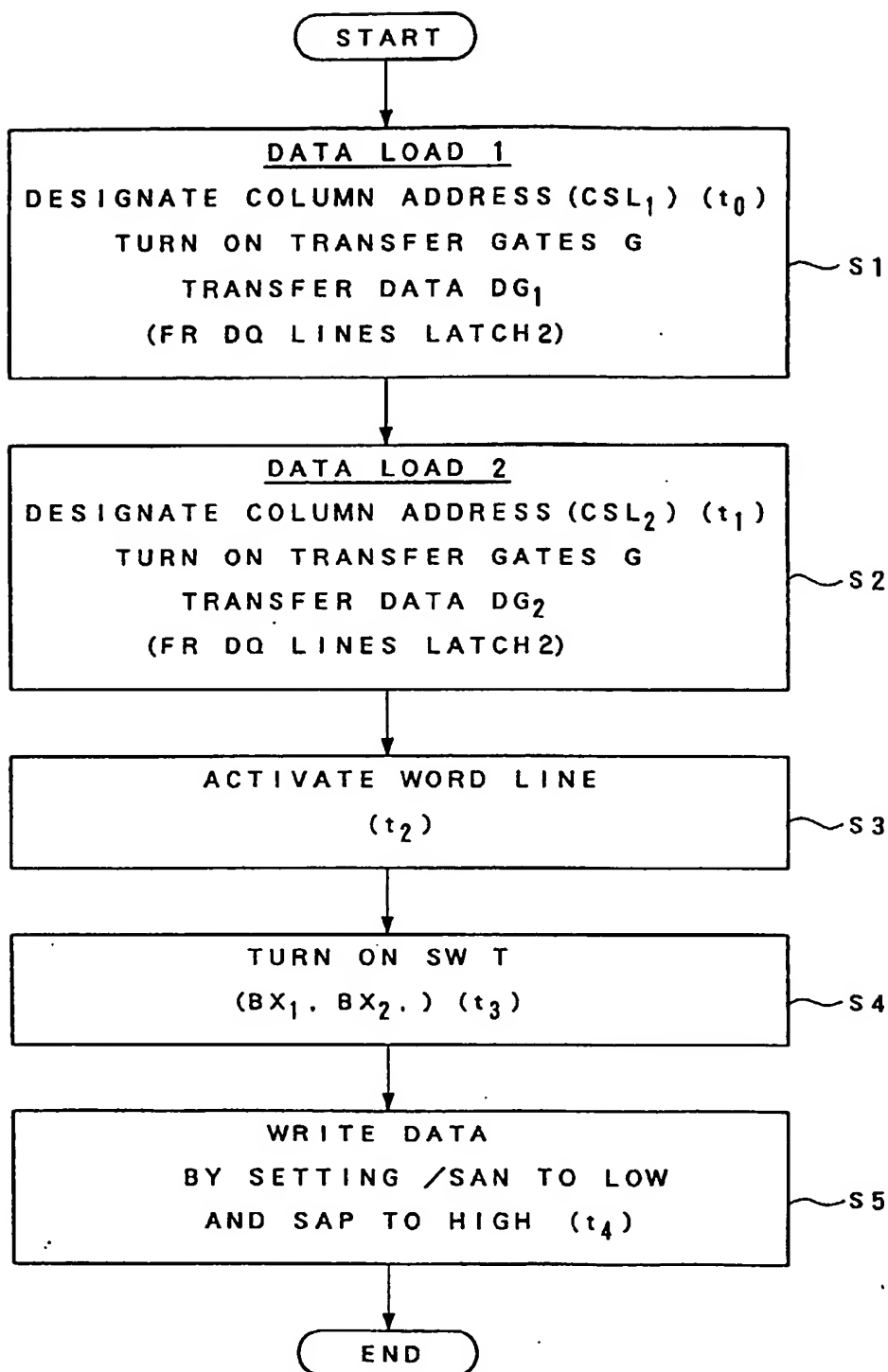


FIG. 2C

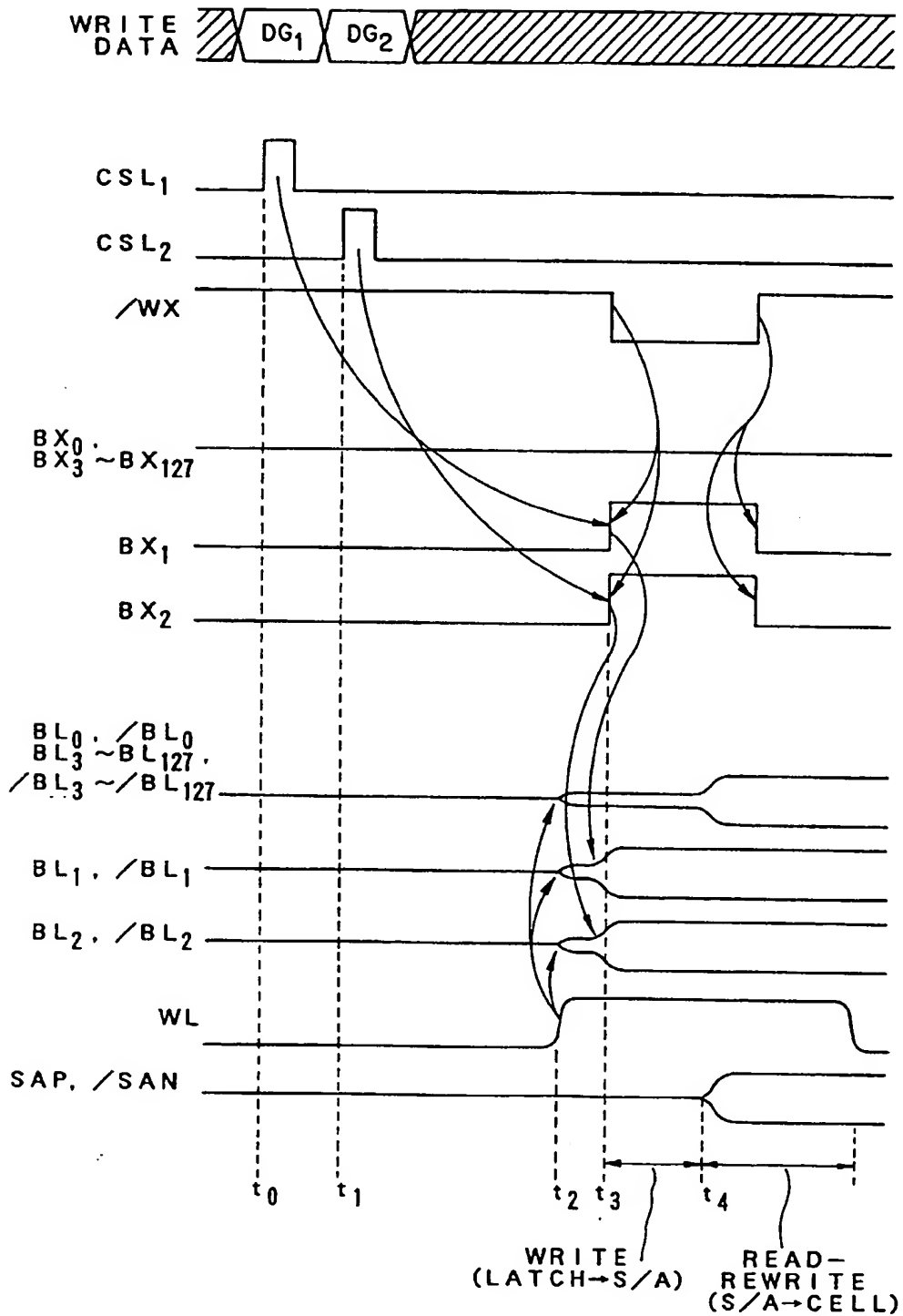


FIG. 2D

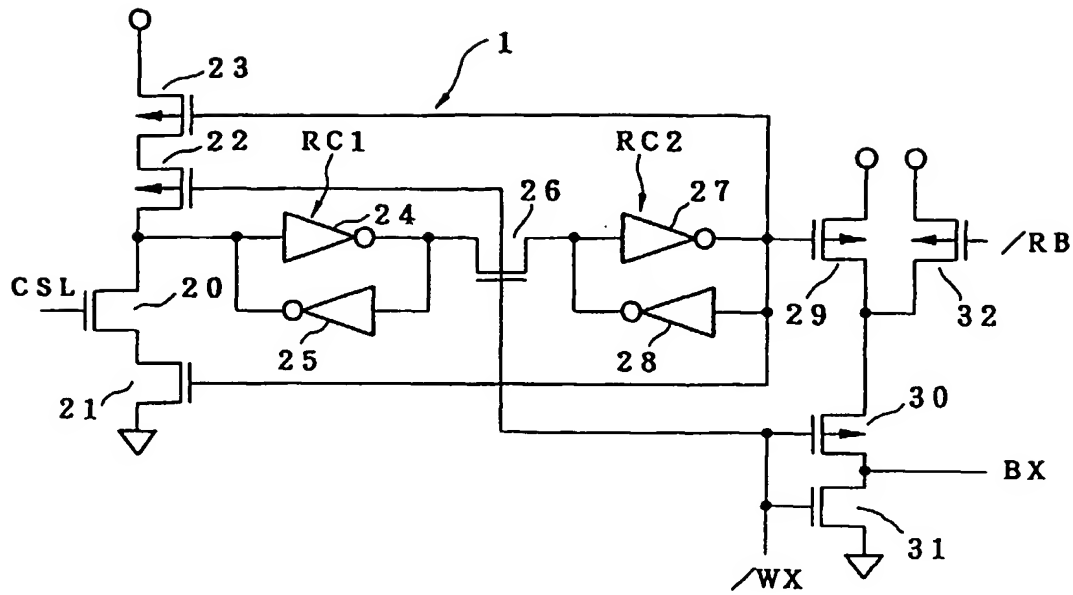


FIG. 3

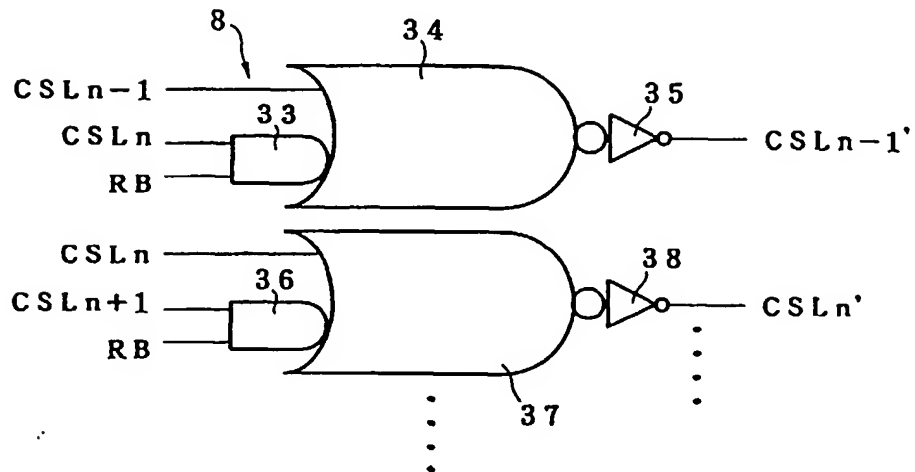


FIG. 4